UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,970	04/13/2004	Hiroyuki Ogawa	AMD-AFO1215	5318

7590 08/12/2005

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
HOANG, QUOC DINH	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/823,970	OGAWA ET AL.	
	Examiner	Art Unit	
	Quoc D. Hoang	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *16-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 1-15) in the reply filed on 06/09/2005 is acknowledged.

2. This office action acknowledges receipt of the following items from the Applicant:

- The Claims filed on 04/13/2004.
- The Specification filed on 04/13/2004.
- The Drawing filed on 04/13/2004.
- The Abstract filed on 04/13/2004.
- The Oath/declaration filed on 04/13/2004.

Oath/Declaration

3. The Oath/declaration filed on 04/13/2004 is acceptable.

Specification

4. The specification has been checked to the extent necessary to determine the present of all possible minor errors. However, Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujiki et al., (US Pat No. 6,607,937) (hereinafter "Fujiki").

Regarding claim 1, Fujiki teaches a semiconductor device 20 comprising:

a pad metal layer 6 having a perimeter area and a center area (col. 9, lines 1-35 and Figs. 1-3). Noted that the second metal wiring 6 is considered the pad metal layer and the perimeter area of the pad metal layer 6 is considered the area that is covered by passivation film 7, which can see in Fig. 3;

a lower metal layer 3 having a plurality of apertures 13 below said center area of said pad metal layer 6 (col. 9, lines 1-35 and Figs. 1-3). Noted that the first metal wiring 3 is considered the lower metal layer, and the slit portions 13 are considered the plurality of apertures; and

an interlayer dielectric 4 formed between said pad metal layer 6 and said lower metal layer 3 (col. 9, lines 1-35 and Figs. 1-3).

Regarding claim 2, Fujiki teaches a plurality of vias 5 formed in said interlayer dielectric 4, wherein said vias electrically couple said pad metal layer 6 and said lower

metal layer 3, and wherein said vias 5 are located below said perimeter area of said pad metal layer 6 (col. 4, lines 25-42, col. 9, lines 1-35 and Figs. 1-3).

Regarding claim 9, Fujiki teaches a semiconductor device 20 comprising:

a pad metal layer 6 having a perimeter area and a center area (col. 9, lines 1-35 and Figs. 1-3). Noted that the second metal wiring 6 is considered the pad metal layer and the perimeter area of the pad metal layer 6 is considered the area that is covered by passivation film 7, which can see in Fig. 3;

a lower metal layer 3 having a plurality of apertures 13 below said center area of said pad metal layer 6 (col. 9, lines 1-35 and Figs. 1-3). Noted that the first metal wiring 3 is considered the lower metal layer, and the slit portions 13 are considered the plurality of apertures;

an interlayer dielectric 4 formed between said pad metal layer 6 and said lower metal layer 3 (col. 9, lines 1-35 and Figs. 1-3); and

a plurality of vias 5 formed in said interlayer dielectric 4, wherein said vias electrically couple said pad metal layer 6 and said lower metal layer 3, and wherein said vias 5 are located below said perimeter area of said pad metal layer 6 (col. 4, lines 25-42, col. 9, lines 1-35 and Figs. 1-3).

7. Claims 6, 7, 13 and 14 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Fujiki et al., (US Pat No. 6,607,937) (hereinafter "Fujiki").

Regarding claim 6, Fujiki fails to teach wherein **a probing process** is performed on said center area of said pad metal layer. Although the Fujiki does not teach wherein a probing process is performed on said center area of said pad metal layer, the present of the process limitations on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephen 145 USPQ 656 (CCPA 1965).

Regarding claim 7, Fujiki fails to teach wherein **a wire-bonding process** is performed on said center area of said pad metal layer. Although the Fujiki does not teach wherein a wire-bonding process is performed on said center area of said pad metal layer, the present of the process limitations on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephen 145 USPQ 656 (CCPA 1965).

Regarding claim 13, Fujiki fails to teach wherein **a probing process** is performed on said center area of said pad metal layer. Although the Fujiki does not teach wherein a probing process is performed on said center area of said pad metal layer, the present of the process limitations on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephen 145 USPQ 656 (CCPA 1965).

Regarding claim 14, Fujiki fails to teach wherein **a wire-bonding process** is performed on said center area of said pad metal layer. Although the Fujiki does not teach wherein a wire-bonding process is performed on said center area of said pad metal layer, the present of the process limitations on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephen 145 USPQ 656 (CCPA 1965).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

9. Claims 3-5, 8, 10-12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiki et al., (US Pat No. 6,607,937) (hereinafter "Fujiki") in view of Heim., (US Pat No. 5,248,903).

Regarding claim 3, Fujiki teaches wherein vias are filled with electrical conductive component (col. 4, line 52-58), but fails to teach wherein the vias are filled with tungsten.

However, Heim teaches wherein the vias 212 are filled with tungsten (col. 4, line 4-6 and Fig. 2A). Since Fujiki and Heim are all from the same field of endeavor, the

purpose disclosed by Heim would have been recognized in the pertinent art of Fujiki. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to fill the vias of Fujiki with tungsten of Heim in order to provide a high electrically conductive vias between the top and bottom bond pads.

Regarding claim 4, Fujiki fails to teach wherein the vias are positioned in a ring arrangement below the pad metal layer.

However, Heim teaches wherein the vias 212 of filled 216 are positioned in a ring arrangement below the pad metal layer 214 (col. 3, line 67 through col. 4, line 57 and Figs. 2A-2B). Since Fujiki and Heim are all from the same field of endeavor, the purpose disclosed by Heim would have been recognized in the pertinent art of Fujiki. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide vias in a ring arrangement below the pad metal layer in order to desirable improve in both assembly (packaging) yield and device reliability as taught by Heim, column 5, lines 10-14.

Regarding claim 5, Fujiki teaches a passivation film 7 that covers said perimeter area of said pad metal layer (see Fig. 3), but fails to teach the passivation film is an insulating dielectric layer.

However, Heim teaches the passivation film 218 is an insulating dielectric layer (col. 4, lines 7-9 and Fig. 2A, borophosphosilicate glass). Since Fujiki and Heim are all from the same field of endeavor, the purpose disclosed by Heim would have been

recognized in the pertinent art of Fujiki. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the passivation film as an insulating dielectric layer in order to provide the contact area on the top surface of the metal pad layer as taught by Heim, column 4, lines 10-20.

Regarding claim 8, Fujiki fails to teach wherein said semiconductor device is an integrated circuit chip.

However, Heim teaches wherein the semiconductor device 200 is an integrated circuit chip (col. 1, lines 6-8, col. 4, lines 14-17 and Fig. 2A). Since Fujiki and Heim are all from the same field of endeavor, the purpose disclosed by Heim would have been recognized in the pertinent art of Fujiki. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide semiconductor device (bond pad) in an integrated circuit chip in order to provide external connections to the chip or die as taught by Heim, column 4, lines 13-17.

Regarding claim 10, Fujiki teaches wherein vias are filled with electrical conductive component (col. 4, line 52-58), but fails to teach wherein the vias are filled with tungsten.

However, Heim teaches wherein the vias 212 are filled with tungsten (col. 4, line 4-6 and Fig. 2A). Since Fujiki and Heim are all from the same field of endeavor, the purpose disclosed by Heim would have been recognized in the pertinent art of Fujiki. It would have been obvious to a person of ordinary skill in the art at the time of the

invention was made to fill the vias of Fujiki with tungsten of Heim in order to provide a high electrically conductive vias between the top and bottom bond pads.

Regarding claim 11, Fujiki fails to teach wherein the vias are positioned in a ring arrangement below the pad metal layer.

However, Heim teaches wherein the vias 212 of filled 216 are positioned in a ring arrangement below the pad metal layer 214 (col. 3, line 67 through col. 4, line 57 and Figs. 2A-2B). Since Fujiki and Heim are all from the same field of endeavor, the purpose disclosed by Heim would have been recognized in the pertinent art of Fujiki. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide vias in a ring arrangement below the pad metal layer in order to desirable improve in both assembly (packaging) yield and device reliability as taught by Heim, column 5, lines 10-14.

Regarding claim 12, Fujiki teaches a passivation film 7 that covers said perimeter area of said pad metal layer (see Fig. 3), but fails to teach the passivation film is an insulating dielectric layer.

However, Heim teaches the passivation film 218 is an insulating dielectric layer (col. 4, lines 7-9 and Fig. 2A, borophosphosilicate glass). Since Fujiki and Heim are all from the same field of endeavor, the purpose disclosed by Heim would have been recognized in the pertinent art of Fujiki. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the passivation

film as an insulating dielectric layer in order to provide the contact area on the top surface of the metal pad layer as taught by Heim, column 4, lines 10-20.

Regarding claim 15, Fujiki fails to teach wherein said semiconductor device is an integrated circuit chip.

However, Heim teaches wherein the semiconductor device 200 is an integrated circuit chip (col. 1, lines 6-8, col. 4, lines 14-17 and Fig. 2A). Since Fujiki and Heim are all from the same field of endeavor, the purpose disclosed by Heim would have been recognized in the pertinent art of Fujiki. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide semiconductor device (bond pad) in an integrated circuit chip in order to provide external connections to the chip or die as taught by Heim, column 4, lines 13-17.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quoc Hoang whose telephone number is (571) 272-1780. The examiner can normally be reached on Monday-Friday from 8.00 AM to 5.00 PM.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers of the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quoc Hoang

Patent examiner/AU 2818

07/21/2005